response of the InP FET is not as fast as expected from its v/E curve, because the operating drain voltage is relatively small in the normally off FET and the maximum electric field in the channel is less than the 10-kV/cm value required for the InP drift velocity to reach its peak.

To improve the response time of the InP FET, a p-n junction FET or a short-gate FET with $l_g \cong 0.5$ μm is a possibility since it would result in a larger channel field.

Acknowledgment

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References

[1] P. T. Greiling, C. F. Krumm, F. S. Ozdemir, and R. F. Lohr, Jr., "Electron-beam fabricated FET inverter," presented at the Device Research Conf., June 1978.

[2] T. Mizutani, M. Ida, and M. Ohmori, "An 80-ps normally-off GaAs MESFET logic," presented at the First Specialty Conf. Gigabit Logic for Microwave Systems, Orlando, FL, May 1979.

[3] R. E. Lundgren, C. F. Krumm, and R. L. Pierson, "Fast enhancement-mode GaAs MESFET logic," presented at the Device Research Conf., June 1979.

[4] C. Jacoboni, C. Canali, G. Ottariani, and A. Alberigi Quaranta, "A review of some charge transport properties of silicon," *Solid-State Electron.*, vol. 20, pp. 77–89, 1977.

[5] M. A. Littlejohn, J. R. Hauser, and T. H. Glisson, "Velocity-field characteristics of $Ga_{1-x}In_xP_{1-y}As_y$ quaternary alloys," *Appl. Phys. Lett.*, vol. 30, no. 5, pp. 242–244, Mar. 1977.

[6] P. E. Bauhahn, G. I. Haddad, and N. A. Masnari, "Comparison of the hot electron-diffusion rates for GaAs and InP," *Electron. Lett.*, vol. 9 no. 19, pp. 460–461, Sept. 1973.

[7] M. Reiser, "A Two-Dimensional Numerical FET Model for dc, ac, and large-signal analysis," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 35–45, Jan. 1973.

[8] J. Frey and T. Wada, "Mobility, transit time and transconductance in submicron-gate-length M.E.S.F.E.T.S," *Electron. Lett.*, vol. 15, no. 1, pp. 26–28, Jan. 1979.

Determination of the Electrode Capacitance Matrix for GaAs FET's

NICOLAOS G. ALEXOPOULOS, MEMBER, IEEE, JOHN A. MAUPIN, MEMBER, IEEE, AND PAUL T. GREILING, MEMBER, IEEE

***Abstract*—In this paper, a method is presented which provides the electrode capacitance matrix for GaAs FET's. The method incorporates a Green's function, valid for conductors printed on or embedded in a grounded substrate, with the moment method technique. Although calculations for various geometries of printed conductors are considered, emphasis is placed on the computation of self- and mutual-capacitances for the source, gate, drain equivalent circuit of a GaAs FET. As an example, the speed power characteristics of a depletion-mode GaAs FET inverter circuit are examined, as a function of device width, pad and gate length.**

I. Introduction

IN THIS PAPER, an accurate model is developed for the determination of the capacitance matrix of multiple conductors with finite dimensions, printed on or embedded in a grounded dielectric substrate. This model has applications in the optimization of high speed integrated circuits (IC's) for which a precise knowledge of the capacitance matrix for the electrodes is of paramount importance for the device and IC design. In order to maximize the speed and minimize the power of the IC, the electrode capacitance matrix must be computed as a function of device width, contact and gate length. By incorporating this capacitance model in the computer-aided design program SPICE2, the speed–power tradeoff of a GaAs FET inverter circuit has been analyzed, as a function of device dimensions, in order to demonstrate the model's usefulness.

The method given here allows for the computation of the capacitance matrix of a system of N, zero thickness, metallic conductors with finite dimensions (see Fig. 1). The approach utilizes the moment methods technique [1] in conjunction with a Green's function appropriate to the geometry of the problem. In this manner, by employing even–odd mode excitations, the unknown charge on each conductor can be determined, which immediately yields the capacitance matrix. The potential V_i of the ith conductor being known, $i=1,2,3,\cdots,N$ the problem is to solve the following system of integral equations

$$V_i = \sum_{j=1}^{N} \int_{S_j} G\{x_i,y_i;x_j,y_j;z\}\,\sigma_j(x_j,y_j)\,dx_j\,dy_j \qquad (1)$$

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N. G. Alexopoulos is with the Electrical Sciences and Engineering Department, University of California, Los Angeles, CA 90024.

J. A. Maupin is with the Hughes Aircraft Company, El Segundo, CA 90009.

P. T. Greiling is with the Hughes Research Laboratories, Malibu, CA 90265.

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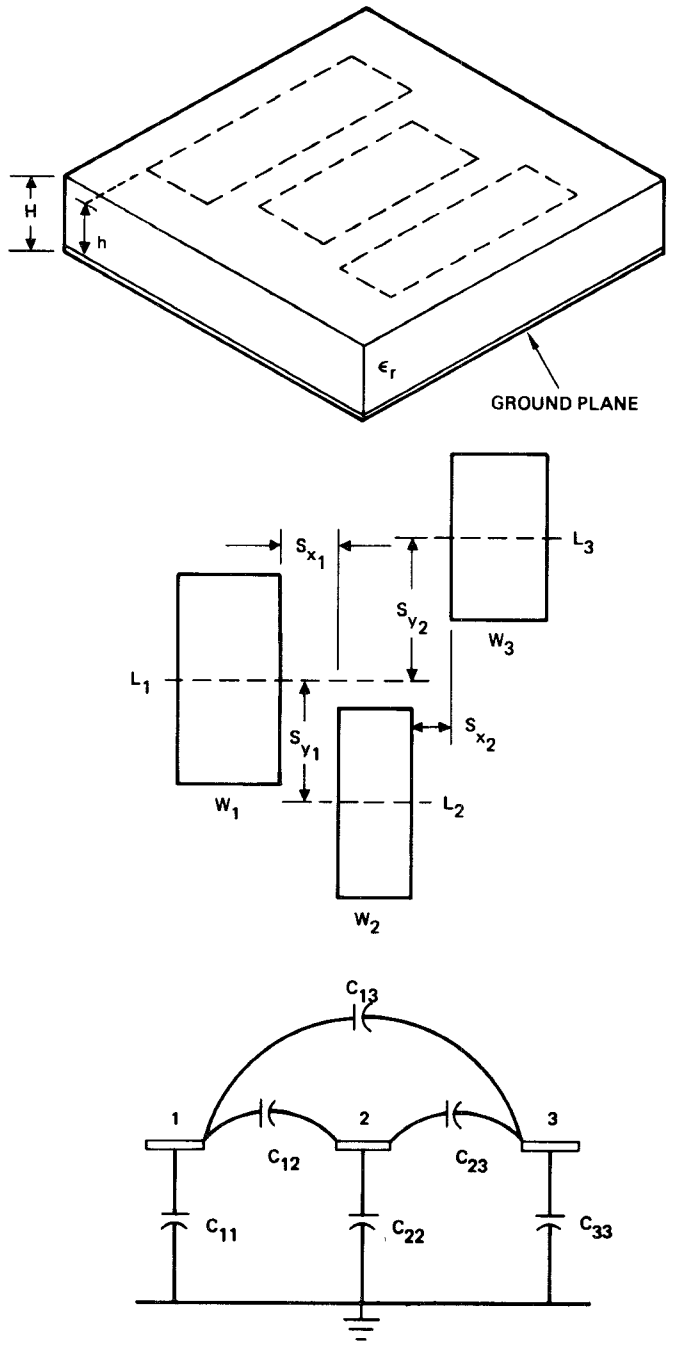

Fig. 1. Three conductor system and equivalent circuit.

where (x_i,y_i), (x_j,y_j) denote coordinate points of the ith and jth conductors, respectively, σ_j is the unknown surface charge density on the jth conductor, $G\{x_i,y_i;x_j,y_j;z\}$ is the Green's function, and S_j is the area of the jth conductor. A solution to this system of equations will yield the unknowns $\sigma_j(x_j,y_j)$ and therefore the total charge of the jth conductor, i.e.,

$$Q_j = \int_{S_j} \sigma_j(x_j,y_j)\,dx_j\,dy_j \tag{2}$$

with $i=1,2,3,\cdots,N$. The capacitance matrix can now be determined by inversion of the system of equations

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \vdots \\ Q_N \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12}\cdots C_{1N} \\ C_{21} & C_{22}\cdots C_{2N} \\ \vdots & \vdots \\ C_{N1} & C_{N2}\cdots C_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \vdots \\ V_N \end{bmatrix} \tag{3}$$

i.e., the partial capacitances are obtained as

$$C_{ij} = \left.\frac{Q_i}{V_j}\right|_{V_i=V_{j-1}=V_{j+1}=\cdots=V_N=0} \tag{4}$$

Moment methods have been adopted in the past to solve the outlined system of equations for infinite printed conductors [2]–[5]. Other techniques, based on the quasi-static approach, have been used very successfully for the two dimensional microstrip problem [6]–[10]. In addition, some results have also been published with respect to the three dimensional problem for related geometries [11]–[20]. However, there has been very little reported work for systems of conductors with finite dimensions embedded in or printed on a grounded dielectric substrate, although the capacitance of a single printed conductor has been previously reported [14].

II. Capacitance of a Single Embedded or Printed Conductor

A single perfectly conducting patch of zero thickness is considered, at first, embedded in the dielectric substrate at a height h above the ground plane. The case of the electrode printed on the substrate results as a limiting situation (i.e., $h\to H$). The conductor is divided into subareas $\Delta S_j, j=1,2,3,\cdots,N$, where $\Delta S_j=\Delta x_j\Delta y_j$. The potential of the ith subarea is V_i, $i=1,2,3,\cdots,N$ and it is given by [14], [15]

$$V_i = \sum_{j=1}^{N} \sigma_j G_{ij} \tag{5}$$

with

$$V_i = \begin{cases} 1, & \text{on conductor surface} \\ 0, & \text{on ground plane} \end{cases}$$

and where G_{ij} is the Green's function pertinent to the problem (see Appendix) while σ_j is the unknown surface charge density of the jth subarea. By rewriting (5) into matrix form and then by inversion, the unknown σ_j can be determined from $[\sigma_j]=[G]^{-1}[V]$, i.e.,

$$\begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \vdots \\ \sigma_N \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12}\cdots G_{1N} \\ G_{21} & G_{2N} \\ \vdots & \vdots \\ G_{N1} & G_{NN} \end{bmatrix}^{-1} \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}. \tag{6}$$

It is a simple matter to compute now the total charge on the conductor, i.e.,

$$Q = \sum_{j=1}^{N} \sigma_j \Delta S_j \tag{7}$$

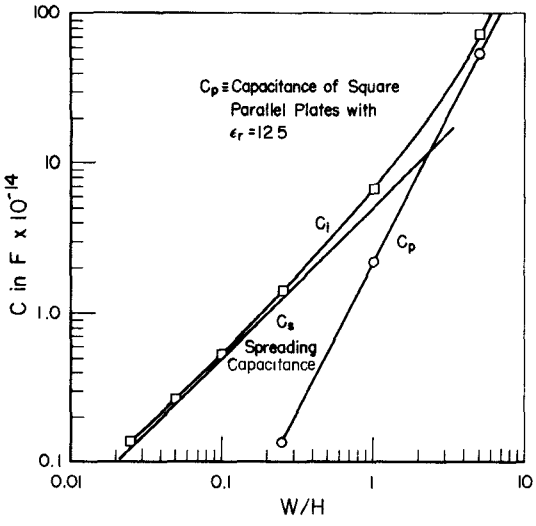

Fig. 2. Capacitance (C_f) of a square printed patch ($H = 200 \times 10^{-6}$ m, $\epsilon_r = 12.5$)

and, therefore, the capacitance

$$C = \frac{Q}{V} = \sum_{j=1}^{N} \sigma_j \Delta S_j = \sum_{i=1}^{N} \sum_{j=1}^{N} D_{ij} \Delta S_j \qquad (8)$$

where D_{ij} is the (i,j)th element of the inverted Green's function matrix. In the employment of the moment methods above, the expansion functions were chosen to be pulse functions constant over each subarea, while impulse functions were selected as weighting functions. Fig. 2 shows the capacitance of a square conductor printed on a GaAs substrate ($\epsilon_r = 12.5$) with $H = 200$ μm. For large $W/H = L/H$ the capacitance approaches that of two large parallel plates filled with GaAs, while for small $W/H = L/H$ it approaches the value of the spreading capacitance C_s. Additional results are presented in Figs. 3 and 4 for a single conductor embedded in and printed on a grounded GaAs substrate, respectively.

III. Several Conductor Geometry

In most practical applications it is necessary to compute the capacitance matrix of a multiple-electrode system. Specifically for GaAs FET modeling, a three conductor system is needed to represent the gate, source, and drain on the surface of the GaAs substrate. The capacitance between pairs of conductors (C_{12}, C_{13}, C_{23}) and between each conductor and ground (C_{11}, C_{22}, C_{33}) can be calculated so that an equivalent circuit model for the FET can be obtained.

In Fig. 1, a three conductor geometry is shown with the corresponding equivalent circuit. The conductor dimensions as well as the spacings are quite arbitrary. In order to compute the capacitances of the equivalent circuit shown in Fig. 1(c), an even–odd mode excitation analysis is used. For the even mode excitation it is assumed that each conductor is at +1 V potential with respect to ground whereas for the odd mode one conductor is at +1 V while the other two are at −1 V potential. That is,

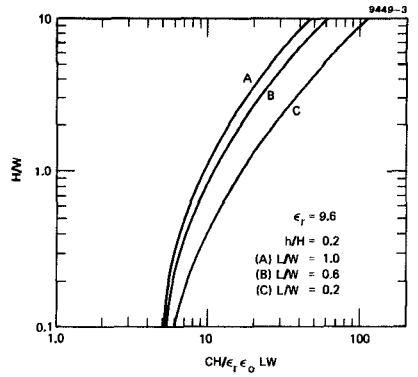

Fig. 3. Single conductor capacitance data for $h/H = 0.2$.

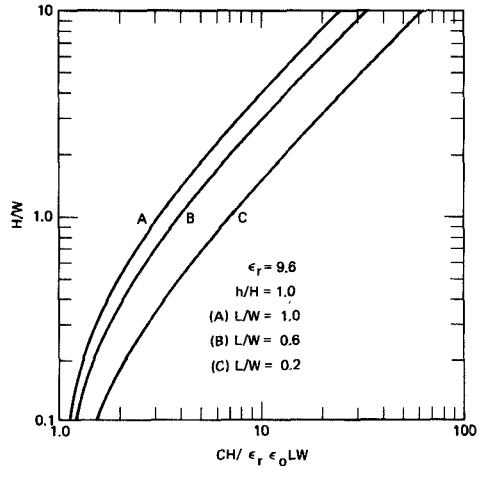

Fig. 4. Single conductor capacitance data for $h/H = 1.0$.

when finding the odd mode charge on the second conductor, for instance, the potentials on the first and third conductors are assumed to be of the opposite sign from the second conductor potential. The capacitance matrix can be computed in this case by computing the even–odd mode capacitances which can be established by considering the symmetries about the magnetic and electric walls for the even and odd modes, respectively. It can be shown that the even–odd mode capacitances are related to the capacitance matrix elements by [15]

$$C_{11} = C_1^{(e)} \qquad C_{22} = C_2^{(e)} \qquad C_{33} = C_3^{(e)} \qquad (9)$$

and

$$C_{12} = \frac{-C_1^{(e)} - C_2^{(e)} + C_3^{(e)} + C_1^{(o)} + C_2^{(o)} - C_3^{(o)}}{4} \qquad (10)$$

$$C_{13} = \frac{-C_1^{(e)} + C_2^{(e)} - C_3^{(e)} + C_1^{(o)} - C_2^{(o)} + C_3^{(o)}}{4} \qquad (11)$$

$$C_{23} = \frac{C_1^{(e)} - C_2^{(e)} - C_3^{(e)} - C_1^{(o)} + C_2^{(o)} + C_3^{(o)}}{4} \qquad (12)$$

where the superscripts (e), (o) refer to even, odd modes correspondingly. The first conductor is divided into N_A subsections, while the second and third conductors are divided into N_B and N_C subsections, respectively. The

total number of subsections is then $N=N_A+N_B+N_C$. The matrix equation for the charge densities is of the form

$$[\sigma]=[G]^{-1}[V]$$

where now

$$[\sigma]=\begin{bmatrix}\sigma_1\\ \sigma_2\\ \vdots\\ \sigma_{N_A}\\ \sigma_{N_A+1}\\ \vdots\\ \sigma_{N_A+N_B}\\ \sigma_{N_A+N_B+1}\\ \vdots\\ \sigma_N\end{bmatrix} \tag{13}$$

and

$$[G]=\begin{bmatrix} G_{1,1} & \cdots G_{1,N_A} & G_{1,N_A+1} & \cdots G_{1,N_A+N_B} & G_{1,N_A+N_B+1} & \cdots G_{1,N}\\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots\\ G_{N_A+1} & \cdots G_{N_A,N_A} & G_{N_A,N_A+1} & \cdots G_{N_A,N_A+N_B} & G_{N_A,N_A+N_B+1} & \cdots G_{N_A,N}\\ G_{N_A+1,1} & \cdots G_{N_A+1,N_A} & G_{N_A+1,N_A+1} & \cdots G_{N_A+1,N_A+N_B} & G_{N_A+1,N_A+N_B+1} & \cdots G_{N_A+1,N}\\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots\\ G_{N_A+N_B,1} & \cdots G_{N_A+N_B,N_A} & G_{N_A+N_B,N_A+1} & \cdots G_{N_A+N_B,N_A+N_B} & G_{N_A+N_B,N_A+N_B+1} & \cdots G_{N_A+N_B,N}\\ G_{N_A+N_B+1,1} & \cdots G_{N_A+ND+1,N_A} & G_{N_A+N_B+1,N_A+1} & \cdots G_{N_A+N_B+1,N_A+N_B} & G_{N_A+N_B+1,N_A+N_B+1} & \cdots G_{N_A+N_B+1,N}\\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots\\ G_{N,1} & \cdots G_{N,N_A} & G_{N,N_A+1} & \cdots G_{N,N_A+N_B} & G_{N,N_A+N_B+1} & \cdots G_{N,N}\end{bmatrix}. \tag{14}$$

The voltage excitation for the even mode of each conductor is a unit column matrix while the respective odd mode excitations yield the following column matrices:

$$[V]_{\text{odd}_1}=\begin{bmatrix}1\\ \vdots\\ -1\\ \vdots\\ -1\\ -1\\ \vdots\\ -1\end{bmatrix} \qquad [V]_{\text{odd}_2}=\begin{bmatrix}-1\\ \vdots\\ -1\\ 1\\ \vdots\\ 1\\ -1\\ \vdots\\ -1\end{bmatrix} \qquad [V]_{\text{odd}_3}=\begin{bmatrix}-1\\ \vdots\\ -1\\ -1\\ \vdots\\ -1\\ 1\\ \vdots\\ 1\end{bmatrix}. \tag{15}$$

By defining again D_{ij} to be the ijth element of the inverted Green's function matrix and by summing separately each of the previously defined nine submatrices there results

$$\begin{aligned} D_1&=\sum_{i=1}^{N_A}\sum_{j=1}^{N_A}D_{ij}\\ D_2&=\sum_{i=1}^{N_A}\sum_{j=N_A+1}^{N_A+N_B}D_{ij}\\ D_3&=\sum_{i=1}^{N_A}\sum_{j=N_A+N_B+1}^{N}D_{ij}\end{aligned} \tag{16}$$

$$\begin{aligned} D_4&=\sum_{i=N_A+1}^{N_A+N_B}\sum_{j=1}^{N_A}D_{ij}\\ D_5&=\sum_{i=N_A+1}^{N_A+N_B}\sum_{j=N_A+1}^{N_A+N_B}D_{ij}\\ D_6&=\sum_{i=N_A+1}^{N_A+N_B}\sum_{j=N_A+N_B+1}^{N}D_{ij}\end{aligned} \tag{17}$$

$$\begin{aligned} D_7&=\sum_{i=N_A+N_B+1}^{N}\sum_{j=1}^{N_A}D_{ij}\\ D_8&=\sum_{i=N_A+N_B+1}^{N}\sum_{j=N_A+1}^{N_A+N_B}D_{ij}\\ D_9&=\sum_{i=N_A+N_B+1}^{N}\sum_{j=N_A+N_B+1}^{N}D_{ij}.\end{aligned} \tag{18}$$

The even and odd mode capacitances can now be determined from the following equation:

$$C_j^{(e,o)}=\frac{Q_j^{(e,o)}}{V_j^{(e,o)}}=\frac{\sum_{i=1}^{N_A}\sigma_i^{(e,o)}\Delta S_j}{V_j^{(e,o)}} \tag{19}$$

where $j=1,2,3$ for the first, second, and third conductors, respectively. The even–odd mode capacitances are given, on the other hand, by

$$\begin{aligned} C_1^{(e)}&=(D_1+D_2+D_3)\Delta S_1\\ C_2^{(e)}&=(D_4{}^{+}D_5+D_6)\Delta S_2\end{aligned} \tag{20}$$

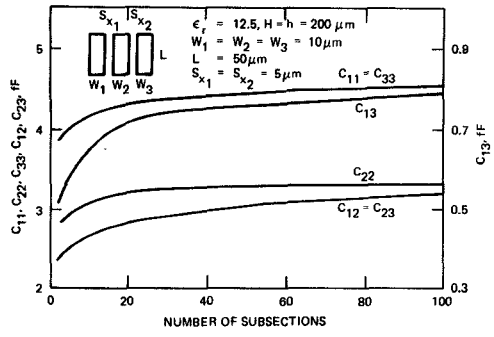

Fig. 5. Three conductor convergence curves.

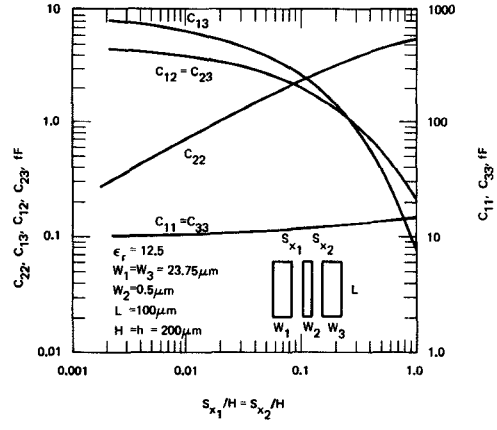

Fig. 6. Three conductor capacitances as a function of spacing.

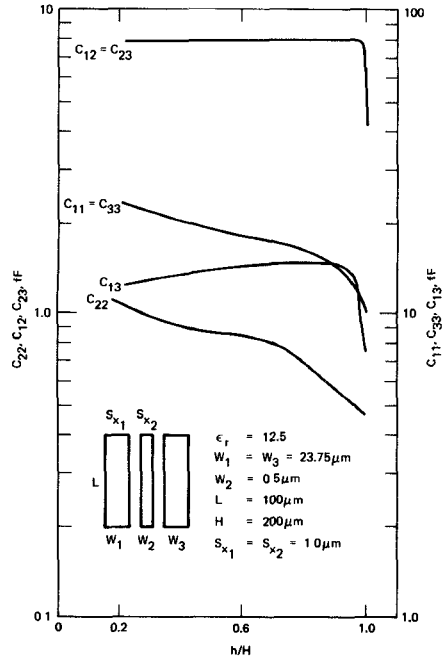

Fig. 7. Three conductor capacitances as a function of conductor level.

$$C_3^{(e)} = (D_7 + D_8 + D_9)\Delta S_3$$
$$C_1^{(o)} = (D_1 - D_2 - D_3)\Delta S_1 \quad (21)$$
$$C_2^{(o)} = (-D_4 + D_5 - D_6)\Delta S_2$$
$$C_3^{(o)} = (-D_7 - D_8 + D_9)\Delta S_3 \quad (22)$$

from which the capacitance matrix elements are determined by considering (9)–(12).

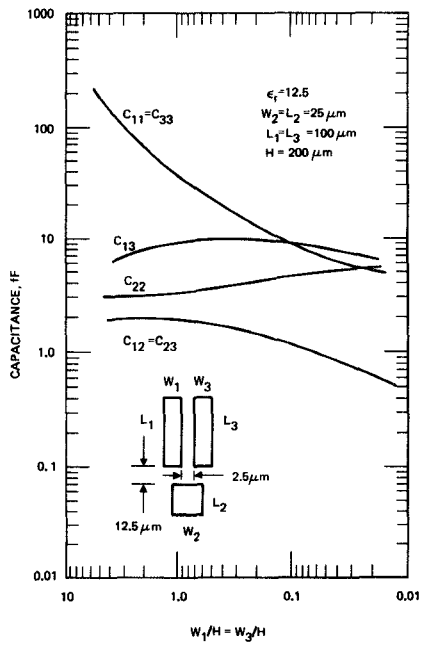

Fig. 8. Three conductor capacitances as a function of width (offset gate).

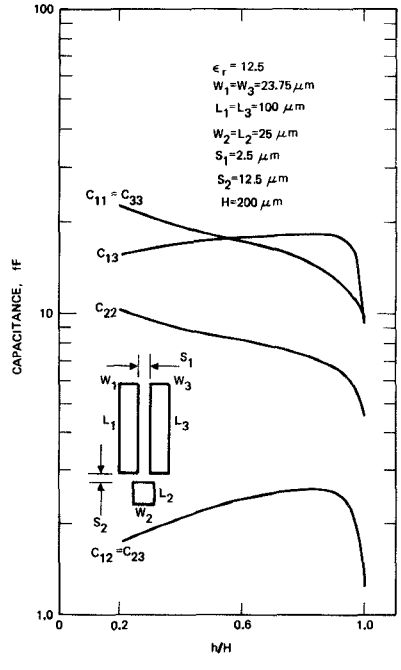

Fig. 9. Three conductor capacitances as a function of conductor level (offset gate).

Obviously, this method can be extended to a system of M conductors, as the same Green's function holds. However, the matrix continues to grow as conductors are added and computer time increases for good accuracy. Computer memory storage is therefore a limitation of this approach as the number of conductors increases. With respect to the three conductor system, there are two geometries of interest in this paper; namely a configuration which represents the source and drain electrodes of a GaAs FET with a gate between them and a second geometry which represents the source and drain electrodes with a gate bonding pad offset from them. Figs. 5–9 show

some representative results for the aforementioned two cases. For each particular situation, specific convergence curves were computed first as shown, e.g., in Fig. 5. The presented results are in general within 2 percent for C_{11}, C_{22}, C_{33} and within 5 percent for C_{12}, C_{23}, C_{13}.

IV. An Application to Speed-Power Tradeoff of a GaAs FET Inverter Circuit

The three conductor system discussed in the previous paragraph is employed now to model the electrode capacitances of a GaAs FET inverter circuit. Device geometry plays an important role in the determination of the speed and power consumption of GaAs IC's. Here, the importance of the FET width and source/drain contact and gate length on the speed and power dissipation is demonstrated by a comparison of the transient performance of the inverter circuit. To this end, an accurate model for the parasitic capacitance of the FET has been used in conjunction with the circuit analysis program SPICE2 to perform a speed power tradeoff analysis of the GaAs FET device. This implies that an optimization of the device dimensions can be affected properly in order that a tradeoff between the current handling capability of the device and the parasitic capacitances can be carried out to maximize the speed and minimize the power of the device [16]. Since the speed of an integrated circuit is determined by the time required to charge and discharge both the device and the circuit parasitic capacitances, the larger the current flowing into and out of the capacitors, the faster the charging and discharging time. The current handling capability and the parasitic capacitances of an FET are directly proportional to the device width, whereas the fringing capacitance at the ends of the device is independent of the device width. Thus as the device width is decreased, the fringing capacitances become a larger portion of the total capacitance of the device. Since the current capability of the FET decreases with decreasing width, the charging time of the parasitic capacitances increases.

In order to optimize GaAs FET IC's, an equivalent circuit model for the FET has been developed which predicts the device dc and transient performance [16]. The parameters of the equivalent circuit model which is incorporated in SPICE2, have been determined from the dc $I-V$ characteristics of the FET. This model scales with device width so that circuits with different size FET's can be analyzed with respect to speed, power consumption, and fan-out capabilities.

An important attribute of this model is that it incorporates accurately the resistance of the FET and the capacitance matrix (i.e., self- and mutual-capacitances). The parasitic resistance has been measured for various FET's with different widths and contact lengths. The capacitance matrix is computed on the basis of the geometry shown on Fig. 10. Since the electronic capacitance of the gate C_{gs} is normally much larger than the interelectrode capacitance C_{12}, C_{gs} is used in the FET model rather than C_{12}.

By incorporating the capacitance model with the circuit

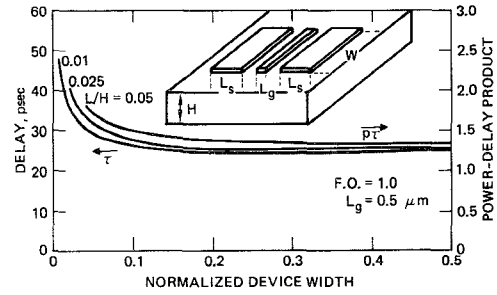

Fig. 10. Delay time and power-delay product as a function of device width ($L_g = 0.5$ μm).

model of the FET, the speed and power consumption of an inverter have been analyzed for different values of fan out as a function of the device geometry. The effect of the device aspect ratio (source/drain width to source/drain length) and the gate length have been investigated in order to optimize their design with respect to speed and power. Van Tuyl and Liechti [17] have shown experimentally that the delay time of an inverter increases for devices whose width is less than 20 to 30 μm. A computer simulation of the transient response of the inverter was performed with the circuit analysis program SPICE2. Variations in device width from 100 μm to 5 μm with aspect ratios from 5–1 to 20–1 were analyzed, including gate lengths of 1 and 0.5 μm. The results of this analysis for an FET with 0.5-μm gate length is shown in Fig. 10. The delay time and the power-delay product are plotted as a function of device width in Fig. 10 for the case of a fan-out of 1. As the device width is decreased below 25 μm for FET's with 10-μm source-and-drain lengths, the delay time increases significantly due to fringing capacitance. By decreasing the source and drain lengths to 2 μm the fringing capacitance decreases and the minimum width of the FET is approximately 10 μm before the delay time increases. The importance of the device geometry as well as the gate length on the circuit speed has been demonstrated by this analysis. Based on these results, the tradeoff between circuit speed and power consumption for high-speed GaAs FET IC's can be made and a circuit can be optimized for either goal.

V. Conclusions

The moments method has been employed in conjunction with the appropriate Green's function to compute the capacitance matrix of a system of three conductors. The conductors have zero thickness, finite width and length, and they may be embedded in or printed on a grounded substrate. This accurate model for device and circuit parasitic capacitances has been adopted to develop an equivalent circuit of a GaAs FET in order to investigate the speed power tradeoff of an inverter circuit.

Appendix

The Green's function is obtained by considering the potential at a point (x_i, y_i, z_i) due to a very small uniformly charged subsection centered at (x_j, y_j, z_j). This potential for the rectangular subsection is given in free space by [14]

$$V(x_i,y_i,z_i)=\frac{1}{4\pi\epsilon_0}\left\{(x_j-x_i)\ln\left[\frac{(c+A')(d+B')}{(d+C')(c+D')}\right]\right.$$
$$+\frac{\Delta x_j}{2}\ln\left[\frac{(d+B')(d+C')}{(c+D')(c+A')}\right]$$
$$+(y_j-y_i)\ln\left[\frac{(a+A')(b+B')}{(b+D')(a+C')}\right]$$
$$+\frac{\Delta y_j}{2}\ln\left[\frac{(b+B')(b+D')}{(a+C')(a+A')}\right]$$
$$-h\left[\tan^{-1}\left(\frac{ac}{hA'}\right)+\tan^{-1}\left(\frac{bd}{hB'}\right)\right]$$
$$\left.+h\left[\tan^{-1}\left(\frac{ad}{hC'}\right)+\tan^{-1}\left(\frac{bc}{hD'}\right)\right]\right.$$

where

$$h=z_j-z_i$$
$$a=x_j-\Delta x_j/2-x_i \qquad b=x_j+\Delta x_j/2-x_i$$
$$c=y_j-\Delta y_j/2-y_i \qquad d=y_j+\Delta y_j/2-y_i$$
$$A'=a^2+c^2+h^2 \qquad B'=b^2+d^2+h^2$$
$$C'=a^2+d^2+h^2 \qquad D'=b^2+c^2+h^2$$

and $\Delta x_j\Delta y_j$ is the area of the jth subsection. When this patch is embedded inside the substrate, image theory is employed which yields for the Green's function, appropriate to the microstrip substrate,

$$G_{ij}\left(x_i,\frac{h}{x_j,h}\right)=\frac{1}{4\pi\epsilon}\sum_{n=1}^{\infty}\left\{(-1)^{n-1}\kappa^n\left[(x_j-x_i)\right.\right.$$
$$\cdot\ln\left[\frac{(c+A'')(d+B'')(d+G'')(c+I'')}{(d+C'')(c+D'')(c+E'')(d+F'')}\right]$$
$$+\frac{\Delta x_j}{2}\ln\left[\frac{(d+B'')(d+C'')(c+E'')(c+I'')}{(c+D'')(c+A'')(d+G'')(d+F'')}\right]$$
$$+(y_j-y_i)\ln\left[\frac{(a+A'')(b+B'')(b+I'')(a+G'')}{(b+D'')(a+C'')(a+E'')(b+F'')}\right]$$
$$+\frac{\Delta y_j}{2}\ln\left[\frac{(b+B'')(b+D'')(a+E'')(a+G'')}{(a+C'')(a+A'')(b+I'')(b+F'')}\right]$$
$$-(2h-2nH)\left(\tan^{-1}\frac{ac}{(2h-2nH)A''}\right.$$
$$\left.+\tan^{-1}\frac{bd}{(2h-2nH)B''}\right)$$
$$+(2h-2nH)\left(\tan^{-1}\frac{ad}{(2h-2nH)C''}\right.$$
$$\left.+\tan^{-1}\frac{bc}{(2h-2nH)D''}\right)$$
$$+(2nH)\left(\tan^{-1}\frac{ac}{2nHE''}+\tan^{-1}\frac{bd}{2nHF''}\right)$$
$$-(2nH)\left(\tan^{-1}\frac{ad}{2nHG''}+\tan^{-1}\frac{bc}{2nHI''}\right)\Big]$$
$$+(-1)^n\kappa^{n-1}\left[(x_j-x_i)\right.$$
$$\cdot\ln\frac{(c+J'')(d+K'')(d+P'')(c+Q'')}{(d+L'')(c+M'')(c+N'')(d+O'')}$$
$$+\frac{\Delta x_j}{2}\ln\frac{(d+K'')(d+L'')(c+N'')(c+Q'')}{(c+M'')(c+J'')(d+O'')(d+P'')}$$
$$+(y_j-y_i)\ln\frac{(a+J'')(b+K'')(b+Q'')(a+P'')}{(b+M'')(a+L'')(a+N'')(b+O'')}$$
$$+\frac{\Delta y_j}{2}\ln\frac{(b+K'')(b+M'')(a+P'')(a+N'')}{(a+L'')(a+J'')(b+O'')(b+Q'')}$$
$$-(2h+(2n-2)H)\left(\tan^{-1}\frac{ac}{(2h+(2n-2)H)J''}\right.$$
$$\left.+\tan^{-1}\frac{bd}{(2h+(2n-2)H)K''}\right)$$
$$+(2h+(2n-2)H)\left(\tan^{-1}\frac{ad}{(2h+(2n-2)H)L''}\right.$$
$$\left.+\tan^{-1}\frac{bc}{(2h+(2n-2)H)M''}\right)$$
$$+(2n-2)H\left(\tan^{-1}\frac{ac}{(2n-2)HN''}+\tan^{-1}\frac{bd}{(2n-2)HO''}\right)$$
$$\left.-(2n-2)H\left(\tan^{-1}\frac{ad}{(2n-2)HP''}+\tan^{-1}\frac{bc}{(2n-2)HQ''}\right)\right]\Big\}$$

where

$$A''=\sqrt{a^2+c^2+(2h-2nH)^2} \qquad B''=\sqrt{b^2+d^2+(2h-2nH)^2}$$
$$C''=\sqrt{a^2+d^2+(2h-2nH)^2} \qquad D''=\sqrt{b^2+c^2+(2h-2nH)^2}$$
$$E''=\sqrt{a^2+c^2+(2nH)^2} \qquad F''=\sqrt{b^2+d^2+(2nH)^2}$$
$$G''=\sqrt{a^2+d^2+(2nH)^2} \qquad I''=\sqrt{b^2+c^2+(2nH)^2}$$
$$J''=\sqrt{a^2+c^2+(2h+(2n-2)H)^2} \qquad K''=\sqrt{b^2+d^2+(2h+(2n-2)H)^2}$$
$$L''=\sqrt{a^2+d^2+(2h+(2n-2)H)^2} \qquad M''=\sqrt{b^2+c^2+(2h+(2n-2)H)^2}$$
$$N''=\sqrt{a^2+c^2+((2n-2)H)^2} \qquad O''=\sqrt{b^2+d^2+((2n-2)H)^2}$$
$$P''=\sqrt{a^2+d^2+((2n-2)H)^2} \qquad Q''=\sqrt{b^2+c^2+((2n-2)H)^2}\ .$$

In addition

$$\kappa = \frac{\epsilon - \epsilon_0}{\epsilon + \epsilon_0}.$$

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REFERENCES

[1] R. F. Harrington, *Field Computation by Moment Methods*. New York: Macmillan, 1968.
[2] A. T. Adams and J. R. Mautz, "Computer solution of electrostatic problems by matrix inversion," in *Proc. 1969 Nat. Electronics Conf.*, pp. 198–201, 1969.
[3] A. T. Adams, *Electromagnetics for Engineers*. New York: Ronald Press, 1971.
[4] N. G. Alexopoulos and N. K. Üzunoglu, "Characteristics of thick microstrip on anisotropic substrates," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 455–456, June 1978.
[5] ——, "An efficient computation of thick microstrip properties on anisotropic substrates," *J. Franklin Inst.*, vol. 36, no. 1, pp. 9–22, July 1978.
[6] T. G. Bryant and J. A. Weiss, "Parameters of microstrip transmission lines and of coupled pairs of microstrip lines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-16, pp. 1021–1027, Dec. 1968.
[7] E. Yamashita, "Variational method for the analysis of microstrip-like transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-16, pp. 529–535, Aug. 1968.
[8] M. V. Schneider, "Microstrip lines for microwave integrated circuits," *Bell Syst. Tech. J.*, pp. 1421–44, May–June 1969.
[9] P. Silvester and P. Benedek, "Electrostatics of the microstrip-Revisited," *IEEE Microwave Theory Tech.*, vol. MTT-20, pp. 756–758, Nov. 1972.
[10] W. T. Weeks, "Calculation of coefficients of capacitance of multiconductor transmission lines in the presence of a dielectric interface," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 35–43, Jan. 1970.
[11] R. A. Pucel, H. A. Haus and H. Statz, "Signal and noise properties of Gallium Arsenide field effect transistors," *Adv. Electron. Electron. Phys.*, vol. 38, pp. 195–264, 1975.
[12] P. D. Patel, "Calculation of capacitance coefficients for a system of irregular finite conductors on a dielectric sheet," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 862–869, Nov. 1971.
[13] A. E. Ruehli and P. A. Brennan, "Capacitance models for integrated circuit metallization wires," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 530–536, Dec. 1975.
[14] A. Farrar and A. T. Adams, "Computation of lumped microstrip capacities by matrix methods-rectangular sections and end-effect," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 495–497, May 1971.
[15] J. A. Maupin, "Self- and mutual-capacitance of printed or embedded patch conductors," Masters thesis, Univ. California, Los Angeles, 1979.
[16] J. A. Maupin, P. T. Greiling, and N. G. Alexopoulos, "Speed Power Tradeoff in GaAs FET Integrated Circuits," presented at 1st Speciality Conf. on Gigabit Logic for Microwave Systems, Orlando, FL, Apr. 30–May 4, 1979.
[17] R. L. Van Tuyl and C. A. Liechti, "Gallium arsenide digital integrated circuits," Tech. Rep. AFAL-TL-74-40, Air Force Avionics Lab. Contract F33615-C-1242, Mar. 1974.

MSI High-Speed Low-Power GaAs Integrated Circuits Using Schottky Diode FET Logic

STEPHEN I. LONG, MEMBER, IEEE, FRANK S. LEE, R. ZUCCA, SENIOR MEMBER, IEEE, BRYANT M. WELCH, MEMBER, IEEE, AND RICHARD C. EDEN

***Abstract*—A new planar high-density (10^{-3} mm^2/gate) GaAs IC technology has been used for fabricating MSI digital circuits containing up to 75 gates/chip. These digital circuits have potential application for gigabit microwave data transmission and processor systems. The circuits consist of Schottky diode FET logic NOR gates, which have provided propagation delays in the 75–200-ps range with dynamic switching energies as low as 27 fJ/gate on ring oscillator structures. Power dissipation levels are compatible with future LSI/VLSI extensions. Operation of *D* flip-flops (*D*FF) as binary ripple dividers (÷2–÷8) was achieved at 1.9-GHz clock rates, and an 8:1 full-data multiplexer and 1:8 data demultiplexer were demonstrated at 1.1-GHz clock rates. This corresponds to equivalent propagation delays in the 100–175-ps range for these MSI circuits. Finally, a 3×3 parallel multiplier containing 75 gates functioned with a propagation delay of 172 ps/gate and with average gate power dissipations of as low as 0.42 mW/gate.**

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The authors are with Rockwell International Electronics Research Center, Thousand Oaks, CA 91360.

I. INTRODUCTION

THE SUCCESSFUL utilization of GaAs for digital integrated circuits has brought about higher speed and lower power logic circuits than were possible with silicon IC approaches. For example, GaAs frequency di-

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